REMARKS

Claims 13, 32, 34, 42, 44, 50, and 52 are amended, no claims are canceled, and no claims are added; as a result, claims 13-16 and 32-60 remain pending in this application.

Drawing Objections

Applicant notes the objection to the drawings lacking reference number 120. Applicant above amends the specification to correct the reference number relating to the data bus to 115. Withdrawal of the objection to the drawings is requested.

The drawings were also objected to as lacking a data in buffer, a data out buffer, a column decoder, and a row decoder for the memory device (i.e., DRAM). Applicant herewith proposes a new Figure 6 showing these features. These features are part of the memory device as set forth in the specification. No new matter is believed proposed. Entry of new Figure 6 is requested.

Specification Objection

Applicant amends the specification, namely, the paragraph beginning on page 8 at line 3, as suggested by the examiner. No new matter is proposed. The specification amendment is supported by the drawings and the disclosure as a whole. Entry of the proposed specification amendment is requested.

Applicant further proposes amendments to specification paragraphs beginning on page 8, lines 18 and 27. Applicant amends these paragraphs to adopt a uniform reference number (115) for the data bus and conform the reference number to the drawings.

Double Patenting Rejection

Claims 13-16 and 32-60 were provisionally rejected under the judicially created doctrine of double patenting over claims 50-54 of copending Application No. 09/434,731. A Terminal Disclaimer will be considered when all claims are indicated to be otherwise allowable.

§112 Rejection of the Claims

Claims 13-16 and 32-60 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully traverses. As described in MPEP § 2164 et seq., the following represents the *prima facie* case that the Examiner must provide in order to maintain a rejection of nonenablement with respect to the disclosure of a patent application under 35 U.S.C. § 112, first paragraph:

1. a rational basis as to
    a. why the disclosure does not teach, or
    b. why to doubt the objective truth of the statements in the disclosure that purport to teach;
2. the manner and process of making and using the invention;
3. that correspond in scope to the claimed invention;
4. to one of ordinary skill in the pertinent technology;
5. without undue experimentation; and
6. dealing with subject matter that would not already be known to the skilled person as of the filing date of the application.

Since the Examiner has not provided evidence supporting each of these elements, the Examiner has not made out a *prima facie* case for nonenablement under 35 U.S.C. § 112, first paragraph.

§103 Rejection of the Claims

Claims 13-16 and 32-60 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Katayama et al. (U.S. Patent No. 5,875,452) in view of Bechtolsheim et al. (U.S. Patent No. 5,270,964). Applicant respectfully traverses.

The examiner admits that Katayama et al. does not specifically mention a data in and a data out buffer (Office Action page 5). It appears that the examiner is relying on his statement that adding additional levels of buffer hierarchies was well known at the time the invention was made to read elements into Katayama that it does not teach. Applicant respectfully traverses this assertion as a form of official notice as the examiner is relying on his assertion that adding levels of buffer hierarchies was well known at the time the invention was made. Applicant requests that the examiner provide a reference that describes such an element. Absent a reference, it appears

that the examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). Applicant respectfully submits that the examiner's reliance on the his belief that adding the additional buffers was well known actually is hindsight. The examiner has not applied any reference that shows all of the features of the present claims. As all of the features are not shown in Katayama et al. or in Bechtolsheim et al., applicant submits that the pending claims are allowable.

Instead, the examiner is modifying Katayama et al. in an attempt to arrive at all of the features of the present claims. However, the justification set forth in the Office Action (page 5) is adding buffers to Katayama would have made timing of the transfer operations to and from the shared buffers more efficient (by latching the data, control or address bits so that protocols as time sharing could be utilized), especially considering the highly parallel nature of Figure 9 embodiment of the Katayama et al system. Applicant requests a basis for this assertion that one of ordinary skill would know that adding buffers would make the Katayama system "more efficient". Adding an additional step, e.g., through a DRAM level buffer and a module level register, in retrieving data from memory might be considered less efficient. Applicant further requests clarification as to the "time sharing" that would be achieved. If a plurality of Katayama et al.'s memory systems were connected to it bus, then it would have the same drawback as described in the present application for conventional memory systems. That is, the load on the buses would be the number of memory devices times the number of memory systems connected to the bus. In contrast, the present invention adds a buffer to each memory system so that the load on the bus is equal to the number of memory systems not the number of memory devices times the number of memory systems.

The Office Action further relies on St. Regis Paper Co. v. Bemis Co., 193 USPQ 8 (7th Cir. 1977) for a position that duplicate parts for multiple effects is not given patentable weight.

Applicant does not see how St. Regis Paper applies to the present claims. First. Applicant requests that the "duplicate parts" relating to the present claims be identified. It appears that the examiner believes adding multiple storage devices 16 of Katayama et al. teaches all of the elements recited in the claims. Applicant respectfully traverses. Specifically, merely adding a plurality of Katayama's storage devices together does not teach or even suggest all of the elements of the claims. Specifically, Katayama does not teach or suggest the pipelined memory subsystems that each have a plurality of memory devices, wherein each contains a data in and a data out buffer, a column decoder and a row decoder, a first register and a second, data register as recited in claim 13. Further, the elements as recited in claim 13 do not rely on merely duplicating parts such as paper bag layers. The present invention as defined by claim 13 includes a plurality of memory subsystems, each connected to a controller through a command and address bus and a data bus. Each of the memory subsystems includes a plurality of memory devices, a command register and a data register. The system of claim 13 does not rely only multiple memory subsystems to distinguish over the art. The present system uses a unidirectional C/A bus and a data bus yet supports a plurality of devices per bus such that the total width of the data path width is not cost prohibitive to manufacture. For example, the present invention provides a memory system which utilizes a single 16-bit data bus which can be operated at 800 MHz and which supports 64 devices. Such a system can also be implemented as a higher bandwidth multiple data bus system as described in the specification. Accordingly, the present invention achieves effects beyond merely duplicating the memory systems. Thus, the corresponding address register and data register result in an effect greater than the sum of the several effects taken separately. For example and as illustrated in Figure 1 of the present application memory system 100 comprises N command and address registers 131, N data registers and N*M DRAMS. Each command and address buffer drives the latched command and address information to its corresponding plurality of memory devices. In this manner, the load on the C/A bus is reduced from N*M devices to only N devices. Additionally, the load on data bus 120 is reduced from N*M devices to only N devices. As a result the effects of the data in and data out buffer of each of the plurality of memory devices, in combination with the address register and the data register within the memory system are more than the sum of the single effects of the internal components of each of

the plurality of memory devices. The addition of an address register coupled between a corresponding plurality of memory devices and a unidirectional command and address bus and a data register coupled between the corresponding plurality of memory devices and a bidirectional data bus results in an embodiment of the present memory system that uses a single 16-bit data bus which can be operated at 800 MHZ and which supports 64 devices. In sum, the present invention as defined by the claims is not obvious under §103. And is certainly not analogous to the courts resolution in St. Regis interpretation of redundancy which found merely adding layers to a paper bag was obvious.

Moreover, Bechtolsheim does not teach or suggest the features not found in Katayama et al.

Based at least on the above, applicant submits that claim 13 is allowable. Claim 14-16 are believed allowable at least because they depend from claim 13.

Referring now to claim 32, applicant comments as follows. Claim 32 recites, in part, latching the data in a data register, driving the latched commands and addresses from the first register to the column and row decoders, driving the latched data to the data in buffers, and storing the data from the data in buffer in the addressable storage of one of the plurality of memory devices. Applicant can not find these features in Katayama or Bechtolsheim. Withdrawal of the rejection of claim 32 and claim 33 depending from claim 32 is respectfully requested.

Referring now to claim 34, applicant believes it is allowable for substantially similar reasons as stated above.

Referring now to claim 36, it recites, in part, wherein the data in buffer receives data information from the data register. Thus, the memory module includes a data register at the module level and a data in buffer at the memory device level. Applicant can not find these features in Katayama or Bechtolsheim. Withdrawal of the rejection of claim 36 and claims 37-39 depending from claim 36 is respectfully requested.

Referring now to claim 42, it recites, in part, latching the data in a data in and out buffer of the one of the plurality of memory devices, latching the data from the data in and data out buffer in a data register associated with the plurality of memory devices, and communicating the

data from the data register, through the data lines, to the data bus. Applicant can not find these features in Katayama or Bechtolsheim. Withdrawal of the rejection of claim 42 and claim 43 depending from claim 42 is respectfully requested.

Referring to claim 44, applicant comments as follows. Applicant amends claim 44 to clarify its recitation of the feature that results from the recited structure of N memory modules each having M memory devices along with a command and address register and a data register for each of the N memory modules. Specifically, the command and address bus and the data bus support N*M memory devices yet only experience a load of N registers. This allows a greater amount of memory without unduly loading the busses connected to the memory. Applicant can not find these features in Katayama or Bechtolsheim. Withdrawal of the rejection of claim 44 and claims 45-47 depending from claim 44 is respectfully requested.

Referring to claim 48, it recites, in part, latching the commands and addresses in a first register, latching the data in a data register, driving the latched commands and addresses to the plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder, driving the latched data to the data in buffers, and storing the data in the addressable storage of one of the plurality of memory devices. Applicant can not find these features in Katayama or Bechtolsheim. Withdrawal of the rejection of claim 48 and claim 49 depending from claim 48 is respectfully requested.

Referring to claim 50, it recites, in part, communicating data from the addressable storage of one of the plurality of memory devices, latching the data in the data out buffer, latching the data from the data out buffer in a data register, and communicating the data, through the socket to the memory controller, on a bidirectional data bus. Applicant can not find these features in Katayama or Bechtolsheim. Withdrawal of the rejection of claim 50 and claim 51 depending from claim 48 is respectfully requested.

Applicant submits that claims 52-55 are allowable for substantially similar reasons as stated above with regard to claim 44.

Claim 56 includes the features of a plurality of memory subsystems each including a first register; a second register; a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer, a column decoder, and a row decoder, wherein the data in

buffer receives data information from the first register and wherein the column decoder and row decoder receive address information from the second register; and a connector. Katayama and Bechtolsheim do not teach a memory having the registers and buffers as recited. Allowance of claim 56 and claims 57-60 depending therefrom is requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 15 day of July, 2002.

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Signature

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Docket No. 303.306US4
WD # 402381

Micron Ref. No. 96-0214.03

CLEAN VERSION OF PENDING CLAIMS

PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS
Applicant: Kevin J. Ryan
Serial No.: 09/434,654

Claims 13-16 and 32-60, as of July 15, 2002 (Date of Response to Second Office Action).

13. (Amended) A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a plurality of N memory modules, wherein each of the memory modules includes:

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

a first register connected between the command and address bus and the plurality of memory devices, the first register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a second, data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the data in buffers of the plurality of memory devices for a write operation, the data register receiving and latching the data information from the data out buffers of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation;

a socket adapted to receive the memory module and to couple the memory module to the unidirectional command and address bus and to the bidirectional data bus; and

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wherein a first load on the command and address bus is equal to N devices and a second load on the data bus is equal to N devices where the total number of memory devices is N*M.

~~14.~~ 2 The memory system according to claim ~~13~~ 1 wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the first register of the memory module and a second delay introduced by the data register of the memory module.

~~15.~~ 3 The memory system according to claim ~~13~~ 1 wherein each memory device is a dynamic random access memory device.

~~16.~~ 4 The memory system according to claim ~~13~~ 1 wherein M equals 8.

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~~32.~~ 5 (Amended) A method of storing data in a pipelined memory system, wherein the pipelined memory system includes a memory module, a socket, and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder, and a row decoder, and wherein the socket couples the memory module to a unidirectional command and address bus and to a bidirectional data bus, the method comprising:

inserting the memory module in the socket;

communicating commands and addresses, through the socket to the memory module, on the unidirectional command and address bus;

communicating data, through the socket to the memory module, on the bidirectional data bus;

latching the commands and addresses in a first register;

latching the data in a data register;

driving the latched commands and addresses from the first register to the column and row

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decoders;

driving the latched data to the data in buffers; and

storing the data from the data in buffer in the addressable storage of one of the plurality of memory devices.

~~33.~~ 16 The method of claim ~~32~~ 15, wherein communicating commands and addresses and communicating data includes executing a packet protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

~~34.~~ 17 (Amended) A method of reading data in a pipelined memory system, wherein the pipelined memory system includes a memory module and a socket, wherein the socket couples the memory module to a unidirectional command and address bus and a bidirectional data bus, the method comprising:

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inserting the memory module in the socket;

communicating commands and addresses, through the socket to the memory module, on the unidirectional command and address bus;

latching the commands and addresses in a first register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder;

communicating data from the addressable storage of one of the plurality of memory devices;

latching data in the data in and a data out buffer;

latching the data in a data register; and

communicating the data, through the socket to a memory controller, on the bidirectional data bus.

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~~35.~~ 8 The method of claim ~~34~~ 7, wherein communicating commands and addresses and receiving data includes executing a packet protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

~~36.~~ 9 A memory module comprising:

a data register;

a first register;

a plurality M of memory devices, wherein each memory device internally contains a data in and a data out buffer, and further contains a column decoder and a row decoder, wherein the data in buffer receives data information from the data register and wherein the column decoder and row decoder receive address information from the first register; and

a connector, wherein the connector includes command and address lines coupled to the first register and data lines coupled to the data register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus.

~~37.~~ 10 The memory module of claim ~~36~~ 9, wherein the address information and the data information are communicated according to a packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

~~38.~~ 11 The memory module of claim ~~36~~ 9, wherein each memory device is a dynamic random access memory device.

~~39.~~ 12 The memory module of claim ~~36~~ 9, wherein M equals 8.

~~40.~~ 13 A method of storing data in a memory module having a connector, wherein the connector includes command and address lines coupled to a first register and data lines coupled to a data register, wherein the connector is capable of being connected through a socket to a unidirectional

command and address bus and a data bus, the method comprising:

coupling the connector to the socket;

receiving commands and addresses, through the command and address lines, from the unidirectional command and address bus;

receiving data, through the data lines, from the data bus;

latching the commands and addresses in the first register;

latching the data in a data register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage;

driving the latched data to the plurality of memory devices; and

storing the data in the addressable storage of one of the plurality of memory devices.

~~41.~~ 14 The method of claim ~~40~~ 13, wherein the commands and addresses and the data is communicated according to a packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

~~42.~~ 15 (Amended) A method of reading data in a memory module having a connector, wherein the connector includes command and address lines coupled to a first register and data lines coupled to a data register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus, the method comprising:

coupling the connector to the socket;

receiving commands and addresses, through the command and address lines, from the unidirectional command and address bus;

latching the commands and addresses in a first register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage;

reading data from the addressable storage of one of the plurality of memory devices;

latching the data in a data in and out buffer of the one of the plurality of memory devices;

latching the data from the data in and data out buffer in a data register associated with the plurality of memory devices; and

communicating the data from the data register, through the data lines, to the data bus.

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~~43.~~ The method of claim ~~42~~, wherein the commands and addresses and the data is communicated according to a packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

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~~44.~~ (Amended) An electronic system comprising:

a microprocessor;

a memory controller coupled to the microprocessor;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a plurality of N memory modules, wherein each of the memory modules includes:

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer;

a first register connected between the command and address bus and the plurality of memory devices, the first register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the data in buffers of the

plurality of memory devices for a write operation, the data register receiving and latching the data information from the data out buffers of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation;

a plurality of sockets adapted to receive the plurality of memory modules and to couple each memory module to the unidirectional command and address bus and to the bidirectional data bus; and

wherein each of the command and address bus and the data bus support N*M memory devices and only experience a load of N registers.

18 17
~~45.~~ 1 The electronic system of claim ~~44~~ 1, wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the first register of the memory module and a second delay introduced by the data register of the memory module.

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~~46.~~ 1 The electronic system of claim ~~44~~ 1, wherein each memory device is a dynamic random access memory device.

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~~47.~~ 1 The electronic system of claim ~~44~~ 1, wherein M equals 8.

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~~48.~~ 1 In an electronic system having a memory controller, a memory module, wherein the memory module includes a plurality of memory devices, and a socket, wherein the socket couples the memory module to a unidirectional command and address bus and a bidirectional data bus, a method of storing data in one of the plurality of memory devices comprising:

inserting the memory module in the socket;

communicating information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses to the unidirectional command and address bus;

communicating the commands and addresses from the unidirectional command and address bus, through the socket, to the memory module;

communicating data from the memory controller to the bidirectional data bus;

communicating the data from the bidirectional data bus to the memory module;

latching the commands and addresses in a first register;

latching the data in a data register;

driving the latched commands and addresses to the plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder;

driving the latched data to the data in buffers; and

storing the data in the addressable storage of one of the plurality of memory devices.

~~49.~~ 22 The method of claim ~~48~~ 21, wherein communicating commands and addresses and communicating data includes executing a pipeline packet protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

~~50.~~ 23 (Amended) In an electronic system having a memory controller, a memory module, wherein the memory module includes a plurality of memory devices, and a socket, wherein the socket couples the memory module to a unidirectional command and address bus and a bidirectional data bus, a method of reading data from one of the plurality of memory devices comprising:

inserting the memory module in the socket;

communicating information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses to the unidirectional command and address;

communicating the commands and addresses from the unidirectional command and address bus, through the socket, to the memory module;

latching the commands and addresses in a first register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder;

communicating data from the addressable storage of one of the plurality of memory devices;

latching the data in the data out buffer;

latching the data from the data out buffer in a data register; and

communicating the data, through the socket to the memory controller, on a bidirectional data bus.

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51. The method of claim 50, wherein communicating commands and addresses and receiving data includes executing a pipeline packet protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

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52. (Amended) A memory system, comprising:

a unidirectional command and address bus in electrical communication with a memory control device;

a bidirectional data bus in electrical communication with the memory control device;

a plurality of N memory modules, wherein each of the memory modules includes:

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer;

a first register connected between the command and address bus and the plurality of memory devices, the first register receiving and latching commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the

bidirectional data bus, the data register receiving and latching data information from the bidirectional data bus and driving the data information to the data in buffers of the plurality of memory devices for a write operation, the data register receiving and latching the data information from the data out buffers of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation;

a plurality of sockets adapted to receive the plurality of memory modules and to couple each memory module to the unidirectional command and address bus and to the bidirectional data bus; and

wherein each of the command and address bus and the data bus support N*M memory devices and only experience a load of N registers.

53. (26) The memory system of claim 52 (25), wherein the commands and addresses and the data information communicate using a pipelined packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

54. (27) The memory system of claim 52 (25), wherein each memory device is a dynamic random access memory device.

55. (28) The memory system of claim 52 (25), wherein M equals 8.

56. (29) A memory module having a plurality of pipelined memory subsystems, wherein each pipelined memory subsystem includes:

a first register;

a second register;

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer, a column decoder, and a row decoder, wherein the data in buffer receives data information from the first register and wherein the column decoder and row decoder receive

address information from the second register; and

a connector, wherein the connector includes command and address lines coupled to the second register and data lines coupled to the first register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus.

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~~57.~~ 1 The memory module of claim ~~56~~, wherein the address information and the data information are communicated according to a packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the second register.

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~~58.~~ 1 The memory module of claim ~~56~~, wherein each memory device is a dynamic random access memory device.

32 29
~~59.~~ 1 The memory module of claim ~~56~~, wherein M equals 8 and the number of memory subsystems equals two.

33 29
~~60.~~ 1 The memory module of claim ~~56~~, wherein M equals 8 and the number of memory subsystems equals one.

CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS
Applicant: Kevin J. Ryan
Serial No.: 09/434,654

The paragraph beginning at page 8, line 3 is amended as follows:

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Each memory subsystem 130 includes a C/A buffer register 131, a plurality M of memory devices 135 and a data buffer register 141. C/A buffer register 131 receives and latches the command and address information from C/A bus 110. As illustrated in Figure 1, buffer register 131 is connected between the command and address bus 110 and the plurality of memory devices 135.1 through 135.M. In one embodiment, memory system 100 has eight memory subsystems each with eight memory devices 135 (i.e. N times M equals sixty-four). In another embodiment, memory devices 135 are dynamic random access memory devices (DRAMs). The number of memory devices 135 connected to each buffer register 131 may, however, differ from that shown in memory system 100 without departing from the spirit of the present invention.

The two paragraphs beginning at page 8, line 18 are amended as follows:

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Each data register 141 is connected between the plurality of memory devices 135 and data bus 115. For memory read operations, data registers 141 receive and latch data information from memory devices 135. Upon the next clock cycle, data registers 141 provide the information to memory controller 105 by driving the data information on data bus 115. For memory write operations, each data register 141 receives and latches data information from data bus 115. Upon the next clock cycle, data registers 141 drive the data information to their corresponding M memory devices 135. In this manner, the load on data bus 115 is reduced from N*M devices to only N devices.

Each C/A buffer register 131, its corresponding plurality of memory devices 135.1 through 135.M and its corresponding data register 141 define a pipelined memory subsystem 130. Memory subsystems 130.1 through 130.N allow C/A bus 110 and data bus 115 to operate at a significant higher data rate since the loading was reduced by a factor of M. Pipelined memory subsystems 130, however, add a two clock cycle delay to DRAM access. In order to ensure efficient operation, the packet protocol used for communication is defined to incorporate a first delay for C/A buffer register 131 and a second delay for data register 141. Furthermore, memory controller 105 issues command and address packets and data packets in pipeline fashion such that

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the first delay and the second delay do not have a substantial impact on the performance of memory system 100.